

1 Iron Law

- 1.1 For each term in the Iron Law, give at least three techniques that improve that term.

Instructions/program:

Cycles/instruction:

Time/cycle:

- 1.2 Explain how each term changes given the proposed modification (increase / decrease / no effect).

- (a) [Quiz 1, 2011] In a classic RISC pipeline, modify the ISA (and thus the microarchitecture) to use hardware interlocking instead of software interlocking for both branch delay slots and load-use delay slots.

Instructions/program:

Cycles/instruction:

Time/cycle:

- (b) [Quiz 1, 2013] Remove hardware floating-point instructions and instead use software subroutines for floating-point arithmetic

Instructions/program:

Cycles/instruction:

Time/cycle:

2 Pipelining

2.1 Data Hazards: Identify all potential hazards

```

ADDI  x1, x0, 4
SW    x1, 8(x2)
SLLI  x3, x1, 1
ADD   x2, x1, x3
LW    x1, 0(x3)
SUB   x1, x0, x0

```

RAW	WAR	WAW
addi -> sw	sw -> add	addi -> lw

2.2 Structural Hazards

- Are there any structural hazards in a classic 5-stage RISC pipeline?
- Are there any structural hazards in the single-bus microcoded machine?
- What modifications to a RISC pipeline may introduce a structural hazard?

2.3 What does the following code do? How many iterations does it run?

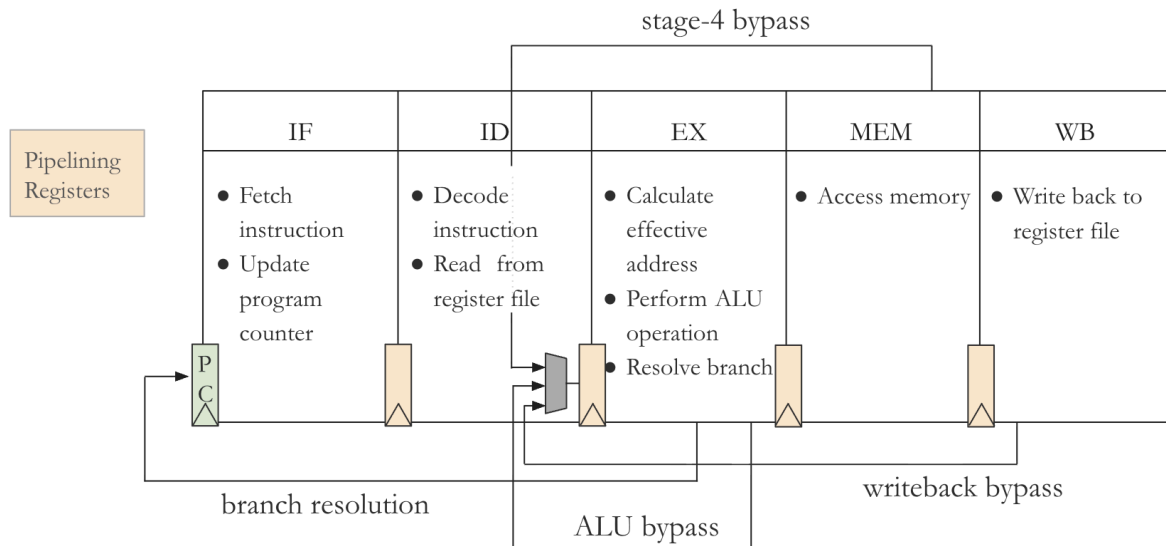
```

        ADDI  x2, x0, 0x700
LOOP:  ADD   x1, x2, x0
        LW    x2, 4(x2)
        BNE  x2, x0, LOOP

```

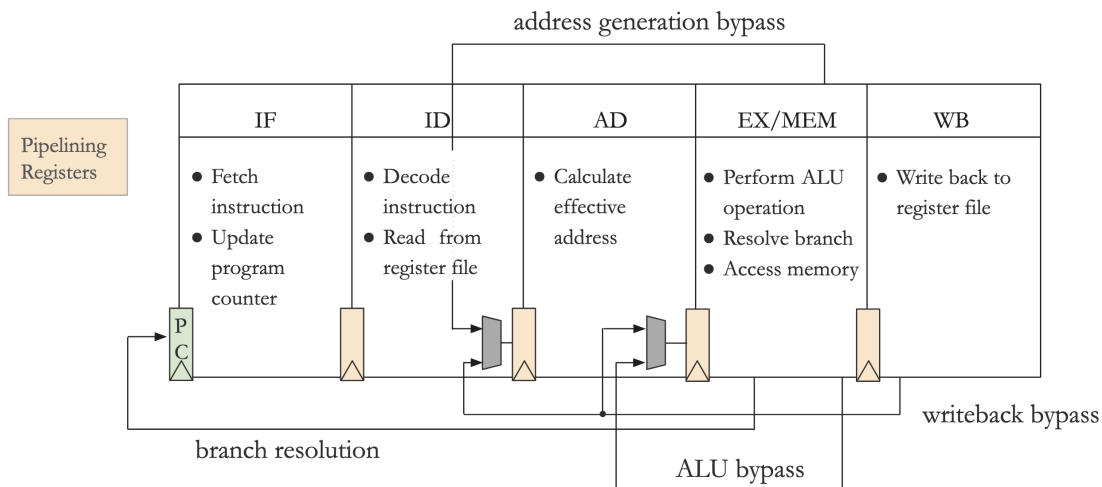
Memory Address	Memory Value
0x400	0x000
0x404	0xD40
...	...
0x700	0x9F0
0x704	0x400
...	...
0x9F0	0x400
0x9F4	0x000
...	...
0xD40	0x000
0xD44	0x9F0

2.4 Using the code from the previous question, fill out the pipeline diagram for the following pipeline, assuming that branches are always predicted not taken.



- What is the CPI for the given code sequence?
- Consider splitting MEM into two stages, M1 and M2. How does the CPI change?
- What is the CPI if the BNE is always correctly predicted?

2.5 Using the same code block, Fill out the pipeline diagram for the following pipeline, assuming that branches are always predicted not taken. [M. Golden and T. Mudge, “A comparison of two pipeline organizations”, 1994]



- What is the CPI for the given code sequence?
- Consider splitting EX/MEM into two stages, M1 and EX/M2. How does the CPI change?
- What is the CPI if bne is always correctly predicted?

2.6 Suppose that the “load-use interlock” (LUI) pipeline from Q2.4 meets timing at 1 GHz. What is the minimum frequency at which the “address-generation interlock” (AGI) pipeline from Q2.5 performs better on the given code sequence, assuming perfect branch prediction?

2.7 Under what circumstances might you consider using the AGI pipeline design over the LUI pipeline?

3 Exceptions

3.1 Why are precise exceptions useful?

3.2 Why might one not want to always implement precise exceptions?