

1 VLIW Dot Product

For the following code block, fill in the VLIW table with instructions.

loop:

```

1: fld f1, 0(x1)
2: fld f2, 0(x2)
3: fmul f3, f1, f2
4: fadd f0, f0, f3
5: addi x1, x1, 8
6: addi x2, x2, 8
7: bne x1, x3, loop

```

Assume the following:

- All FUs fully pipelined
- 1-cycle Integer ALU
- 2-cycle Load/Store Unit
- 3-cycle FP Adder
- 4-cycle FP multiplier
- Perfect branch prediction
- N-cycle latency means that the result is usable in N cycles (i.e., load in cycle 0 is usable in cycle 2)

Label	ALU	MEM	FADD	FMUL
loop	5: addi	1: fld		

