CS152/252A
Spring 2026

Cache Coherence

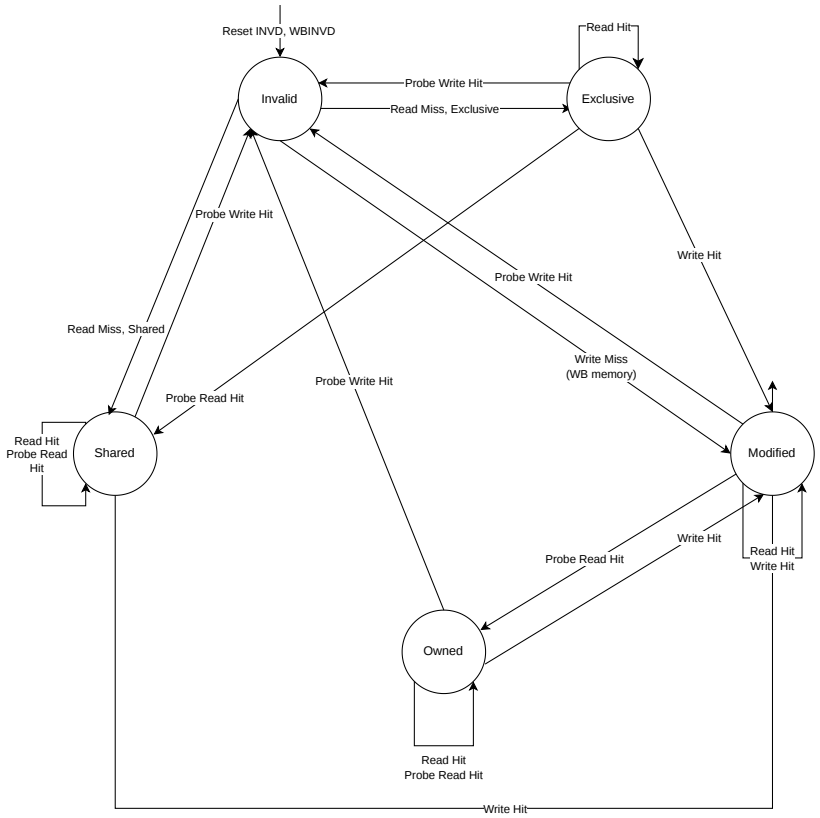
Discussion 10

1 Snooping

1.1 True or False: A snooping cache coherence protocol requires cores to communicate on a single physical bus. Explain your reasoning.

1.2 True or False: In an MSI snooping protocol, a cache line may be in only one of three coherence states.

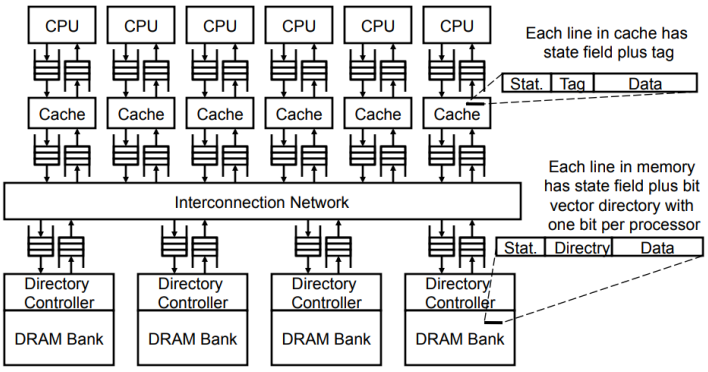
2 MOESI Protocol



2.1 For each of the following new state transitions, indicate whether it is a valid transition. If it is a valid transition, explain what triggers it, what conditions must be true (i.e. do other sharers exist?), and what actions must be taken during the transition.

	Trigger	**Condition**	**Action**
I → O			
O → I			
S → O			
O → S			
E → O			
O → E			
M → O			
O → M			

3 Directory Cache Coherence



In the simplest design, each directory entry contains the state of the cache line and a bit vector with one sharer bit per processor. Assume the directory lines have four states.

How many directory bits are needed per cache line?

3.1 For 128 cores with private caches:

3.2 For 1024 cores with private caches:

3.3 For a 1024-core system with 64-byte cache lines, how many cores must be in each group to reduce the amount of directory state to 10% the amount of physical memory?

3.4 One inefficiency of this system is that you must store directory bits for every line in memory, no matter if it is cached or not. How could you reduce this inefficiency?