

1 Memory Consistency and Caches

1.1 Do memory consistency models apply only to systems with caches?

2 Sequential Consistency

Consider the following two threads executing on two different cores. Memory locations A, B, and C are initialized to zero.

We are interested in the final values of P1.x2, P1.x3, and P2.x2.

	P1:	P2:
	li x1 1	li x1 2
I1	lw x2 A	I1 sw x1 B
I2	sw x1 C	I2 lw x2 C
I3	lw x3 B	I3 sw x1 A

Give all possible sets of values of P1.x2, P1.x3, and P2.x2 and a possible instruction ordering that causes each one.

Instruction Order	P1.x2	P1.x3	P2.x2

3 Relaxing Sequential Consistency

There are four types of ordering constraints:

- (a) Write \rightarrow Read
- (b) Write \rightarrow Write
- (c) Read \rightarrow Write
- (d) Read \rightarrow Read

3.1 Can you think of a microarchitectural optimization made possible by relaxed ordering?

Similarly, there are two flavors of write atomicity relaxation:

- (a) Can a processor see its own write before others?
- (b) Can processor A see some other processor B's writes before they are made visible to the rest of the memory system?

3.2 Can you think of a microarchitectural optimization that would make (a) true?

3.3 Can you think of a microarchitectural optimization that would make (b) true?

4 Weak vs Strong Memory Consistency Models

In general, what is the difference between a weak and a strong memory consistency model? What are the pros and cons of each?

5 Relaxing Ordering Constraints

P1:	P2:
li x1 1	li x1 2
I1 lw x2 A	I1 sw x1 B
I2 sw x1 C	I2 lw x2 C
I3 lw x3 B	I3 sw x1 A

5.1 If we relax Write \rightarrow Read ordering, which instruction(s) can be reordered?

5.2 If we relax Write \rightarrow Read ordering, give the new possible set of values, and a possible instruction ordering that caused said value.

Operation Order	P1.x2	P1.x3	P2.x2

5.3 If we relax Write \rightarrow Write ordering, which instruction(s) can be reordered?

5.4 If we relax Write \rightarrow Write ordering, give the new possible set of values, and a possible instruction ordering that caused said value.

Operation Order	P1.x2	P1.x3	P2.x2

5.5 If we relax Read \rightarrow Read and Read \rightarrow Write ordering, which instruction(s) can be reordered?

5.6 If we relax all orderings, give the new possible set of values, and a possible instruction ordering that caused said value.

Operation Order	P1.x2	P1.x3	P2.x2

6 True/False

Indicate whether the following statements are true or false, and explain why.

6.1 Sequential consistency is guaranteed if all processors have in-order pipelines.

6.2 A high-level language with a sequentially consistent memory model can be implemented on a ISA with a weaker memory model if fence instructions are provided.